High-Yield W-Band Monolithic HEMT Low-Noise Amplifier and Image Rejection Downconverter Chips

Huei Wang, *Member, IEEE*, Kwo Wei Chang, Thuy Nhung Ton, Michael Biedenbender, Sian Tek Chen, Jane Lee, Gee S. Dow, *Member, IEEE*, Kin L. Tan, *Member, IEEE*, and Barry R. Allen, *Member, IEEE*

Abstract—**High-yield W-band monolithic integrated circuits (a three-stage low-noise amplifier (LNA), and a monolithic image rejection downconverter (IRD) using the LNA as the front end followed by an image rejection mixer (IRM)) are discussed. These MMIC's were fabricated in the 0.1-μm AlGaAs–InGaAs–GaAs HEMT production line at TRW. The LNA demonstrated a typical 17-dB gain and 4.5–5.5-dB noise figure at 94 GHz. The complete monolithic IRD has a measured conversion gain of 7–9 dB with a single side-band (SSB) noise figure of 6 dB when downconverting 93–95-GHz RF signal to 50–500 MHz. The downconvertion requires an LO power of 9 dBm. The development of these MMIC's shows the increasing maturity of GaAs based HEMT MMIC technology at W-band.**

I. Introduction

MMIC's provide potential advantages of small size, repeatability and high volume over the conventional hybrid integrated circuit components for many system applications, such as radar, electronic warfare, smart weapon, communication and radiometric systems. A number of W-band (75–110 GHz) MMIC components using HEMT technology have been reported in the past years [1]–[13]. These circuits include LNA's [1]–[6], mixers [4], [7]–[8], voltage control oscillators (VCO's) [9]–[10], a power amplifier (PA) [11], a diode detector [12] and some higher level integration MMIC subsystems such as a downconverter [7], a preamplified detector [12] and a single-chip transceiver [13]. However, the previously reported circuits were fabricated in R&D laboratories and not suitable for volume production. The motivation of this work is to develop high-yield W-band MMIC's using production line process for system applications. From previous experience, the 0.1-μm pseudomorphic (PM) AlGaAs–InGaAs–GaAs HEMT's not only have been proven to yield suitable RF performance at W-band low-noise receivers [5]–[8], [14], but also demonstrated repeatability in MMIC process [15]. Therefore, it was selected as the baseline process for our W-band MMIC production line. A monolithic IRD and its components, namely, a three-stage LNA and an IRM based on this HEMT technology have been designed, fabricated and tested. The IRD has a measured conversion gain of 8 dB with a SSB noise figure of 6 dB when downconverting 93–95-GHz RF signal to 50–500 MHz, driven by an LO power of 9 dBm. An image rejection of greater than 16 dB was achieved, which eliminates the need of a preselect image suppression filter. Total of 256 LNA chips on 16 wafers (3 wafer lots, 16 chips per wafer) from the production line were on-wafer probed for gain and noise figure, demonstrating good yield. The LNA shows a typical measured 17-dB gain and 4.5–5.5 dB noise figure at 94 GHz. The development of these W-band MMIC's shows the increasing maturity of 0.1-μm PM AlGaAs–InGaAs–GaAs MMIC technology.

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The authors are with the Electronic Technology Division, One Space Park, Redondo Beach, CA 90278.

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II. Device Characteristics and MMIC Design

The device structure and the MMIC process has been previously reported [15]. The 0.1-μm T-gate PM HEMT's fabricated in this process typically have a peak dc transconductance G_m of greater than 600 mS/mm with a unity current gain frequency f_T of higher than 100 GHz. The typical minimum noise figure $NF_{\min}$ is about 3 to 3.5 dB at 94 GHz. The planar Schottky diode used in the IRM, with a cutoff frequency of about 450 GHz, is constructed by connecting together the source and drain metals of a HEMT device as the cathode of the diode, while the gate pad is used as the anode. The W-band MMIC design methodology and the HEMT/diode devices modeling procedures were described in [5] and [7].

Fig. 1 shows the block diagram and photograph of the complete monolithic IRD which consists of the three-stage LNA and IRM. The three stage LNA is a two-stage single-ended amplifier cascaded with a single-stage balanced output amplifier. Each stage utilizes a 40-μm HEMT with four gate fingers. The LNA design is similar to the one reported in [5]. The IRM design is a modification of the one reported in [8]. It was constructed using two single-balanced diode mixers, a Lange coupler, and a Wilkinson power divider. The RF and LO signals are in quadrature and in phase, respectively. The 90° Lange coupler is used for the RF port to achieve good input return loss. The overall monolithic IRD is constructed by joining the LNA and IRM with 50-Ω microstrip line including a dc blocking MIM capacitor. Compared with the IRD reported in [14], which was constructed by two separated MMIC chips, the LNA in this design provides twice the output power and

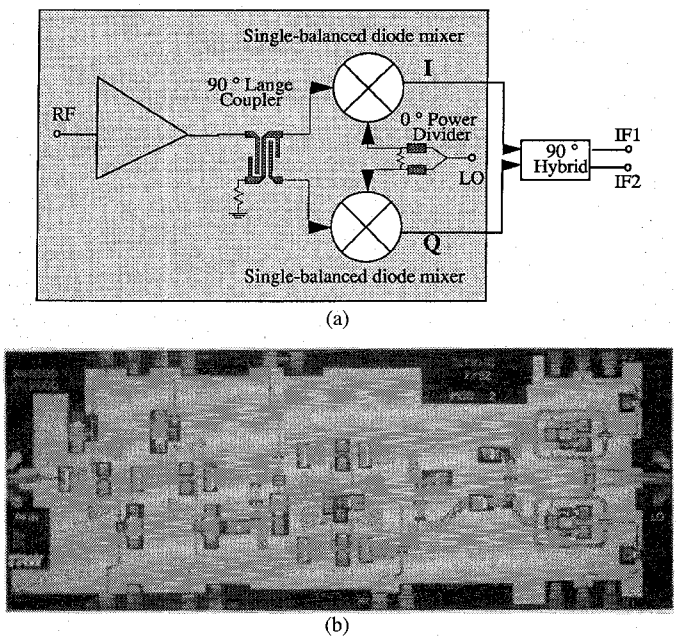

Fig. 1. (a) Block diagram, and (b) photograph, of the W-band monolithic image rejection downconverter. Shaded area in (a) represents the monolithic IRD.

better output VSWR to the mixer owing to the balanced output stage, thus the overall IRD linearity performance is improved and the inter-reflection between two components is reduced. The chip size is 5×2 mm^2.

III. Circuit Measurement Results

The three-stage monolithic LNA's have been measured in test fixture as well as in a W-band on-wafer probe test set [16]. Several chips diced from the first wafer from our production line were measured in a WR10 waveguide fixture. The fixture measurements typically demonstrated a noise figure 5.2 dB and an associated gain of 17 dB at 95 GHz after correction of the waveguide to microstrip line finline transition loss. The drain bias was 2 V for these tests. The total power consumption of this chip was less than 80 mW. Another 256 chips on 16 wafers were tested using the automated W-band on-wafer probe station. The typical measured results of the LNA chips from the on-wafer test set are consistent with the in-fixture testing results. At 94 GHz, the gain runs from 15 to 20 dB and the noise figure varies from 4.2 to 6 dB for most of RF functional chips. The designed noise figure and associated small signal gain of the LNA are 4.7 dB and 17 dB, respectively, at 94 GHz. With this design goal, the LNA demonstrated an RF yield of 56% if 15 dB was used for the gain screening criteria, and 46% for 6 dB noise figure screening criteria. It is noted that the yield data obtained here are the numbers of chips meeting the specification divided by the total numbers of chips being RF tested without dc pre-screening.

The complete IRD was mounted on a fixture and tested with a 3-dB 90° hybrid coupler connecting to its two output ports. The IRD testing procedure is similar to that reported in [14]. The conversion gain and image rejection of the IRD

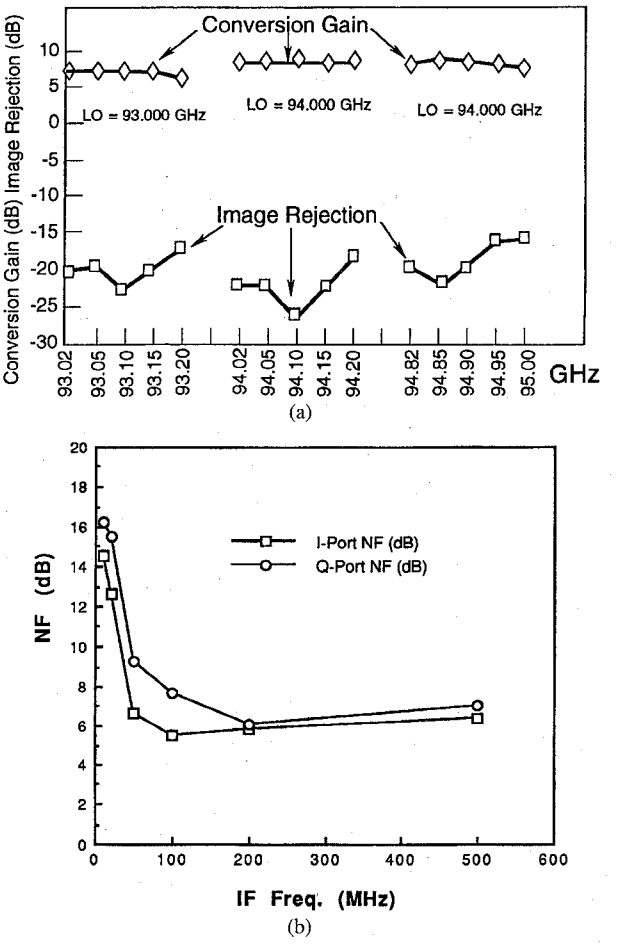

Fig. 2. Measured (a) conversion gain and image rejection vs. RF frequency, (b) I- and Q-port DSB noise figure vs. IF frequency for an LO drive of 9 dBm at 94 GHz, for the monolithic IRD.

vs. various RF and LO frequencies are plotted in Fig. 2(a). The IRD has 7–9-dB conversion gain at RF from 93–95 GHz for the IF from 20–200 MHz with an LO drive of 9 dBm. The image rejection level is better than 16 dB from either I- to Q-port or Q- to I-port. The input power 1-dB compression and noise figure test were also performed. It shows a input power 1-dB compression of -12 dBm. The noise figure of I-port and Q-port vs. IF frequency for 94 GHz LO frequency is plotted in Fig. 2(b). A double side band (DSB) noise figure of 6 dB was observed from 50–500 MHz for both ports. Due to the good image rejection, the DSB and SSB noise figures are within 0.1 dB. The noise figures increase significantly for the IF frequencies below 50 MHz owing to $1/f$ noise of the diode.

IV. Summary

We have presented a W-band monolithic IRD and its components designed and fabricated using our 0.1-μm PM AlGaAs–InGaAs–GaAs HEMT MMIC production line process. Good circuit yield was demonstrated by the statistical testing record of the LNA on three consecutive wafer lots. This result indicates the potential capability of manufacturing W-band MMIC's at low cost.

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